Fundamentals of Gallium Nitride Power Transistors

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The basic requirements for power semiconductors are effciency, reliability, controllability, and cost effectiveness. High frequency capability adds further value in size and transient response in regulators, and fidelity in class D amplifiers. Without effciency and reliability, a new device structure would have no chance of economic viability. There have been many new structures and materials considered; some have been economic successes, others have seen limited or niche acceptance. Recent breakthroughs by EPC in processing Gallium Nitride have produced enhancement mode devices with high conductivity and hyper fast switching, and silicon-like cost structure and fundamental operating mechanism.

Structure

A device's cost effectiveness starts with leveraging existing production infrastructure. EPC's process begins with silicon wafers. Utiilizing existing silicon processing equipment, a thin layer of Aluminum Nitride (AlN) is grown on the Silicon to isolate the device structure from the Substrate. The isolation layer for 200 V and below devices is 300 V. On top of this, a thick layer of highly resistive Gallium Nitride is grown. This layer provides a foundation on which to build the GaN transistor. An electron generating material is applied to the GaN. This layer creates a GaN layer with an abundance of electrons just below it that is highly conductive. Further processing forms a depletion region under the gate. To enhance the transistor, a positive voltage is applied to the gate in the same manner as turning on an n-channel, enhancement mode power MOSFET. A cross section of this structure is depicted in figure 1. This structure is repeated many times to form a power device. The end result is a fundamentally simple, elegant, cost effective solution for power switching. This device behaves similarly to Silicon MOSFETs with some exceptions that will be explained in the following sections.

Operation

EPC's GaN transistors behave very similarly to Silicon Power MOSFETs. A positive bias on the gate relative to the source causes a field effect which attracts electrons that complete a bidirectional channel between the drain and the source. Since the electrons are pooled, as opposed to being loosely trapped in a lattice, the resistance of this channel is quite low. When the bias is removed from the gate, the electrons under it are dispersed into the GaN, recreating the depletion region, and once again, giving it the capability to block voltage.

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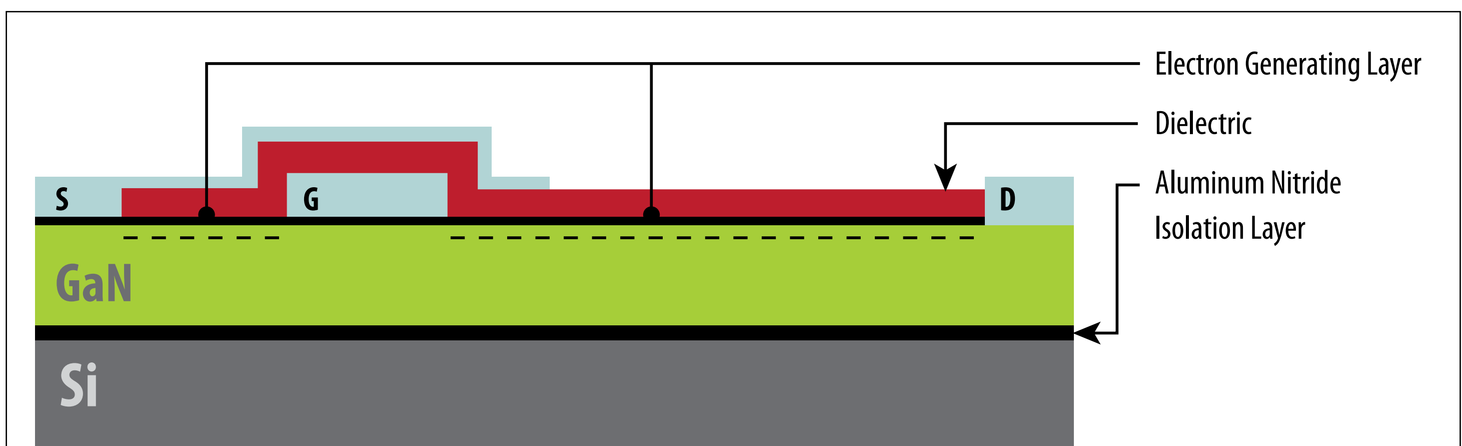


Fig 1 – EPCs' GaN Power Transistor Structure.

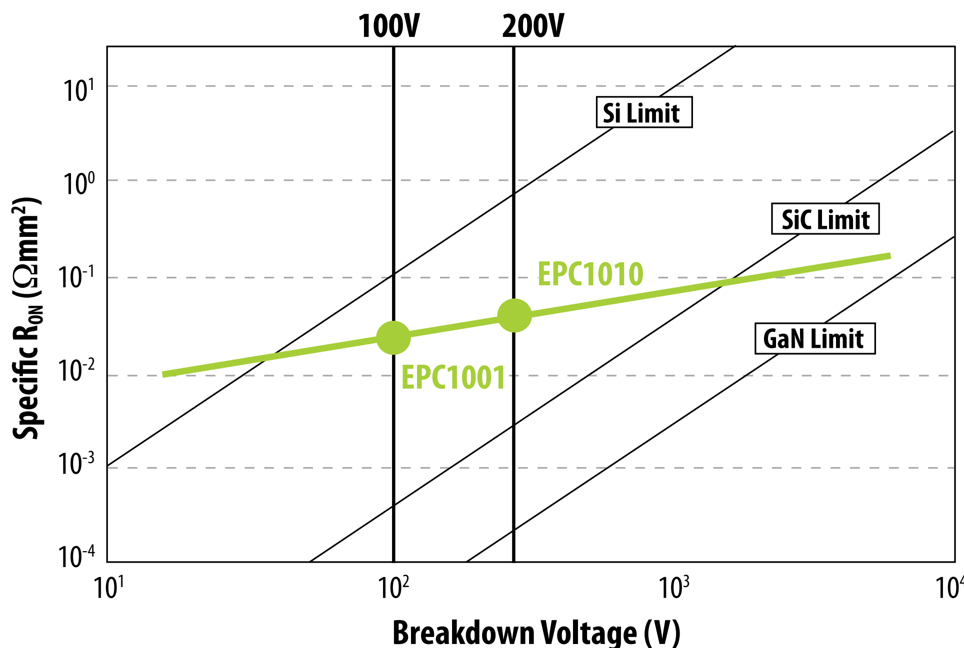


Figure 2: Theoretical resistance times die area limits GaN vs Silicon vs voltage

To obtain a higher voltage device, the distance between the Drain and Gate is increased. As the resistivity of our GaN pool is very low, the impact on resistance by increasing blocking voltage capability is much lower when compared with Silicon. Figure 2 shows the theoretical resistance times die area limits of GaN versus Silicon versus voltage. EPC's first generation of devices is shown as well. Please note that after 30 years of Silicon MOSFET development, it has approached its theoretical limits. Progress in silicon has slowed to the point where small gains have significant development cost. GaN is young in its life cycle, and will see significant improvement in the years to come.

Gate Threshold

The threshold of Gallium Nitride transistors is lower than that of Silicon MOSFETs. This is made possible by the almost flat relationship between threshold and temperature along with the very low C_{GD}, as described later. Figure 3 shows the transfer characteristics curve for the EPC1001, 100V, 5.6 mΩ transistor. Please note the negative relationship between current and temperature. This provides for excellent sharing in the linear region and in diode conduction, which will be explained later. Being that the device starts to conduct significant current at 1.6 V, care must be taken to ensure a low impedance path from gate to source when the device needs to be held off during dV/dt in a rectifier function.

Resistance

$R_{DS(on)}$ versus V_{GS} curves are similar to MOSFETs. EPC first generation GaN transistors are designed to operate with 5 V drive. Figure 4 shows the set of curves for the EPC1001. The curve shows that $R_{DS(on)}$ continues to decrease as the absolute maximum gate voltage is approached. As there is negligible gate drive loss penalty, GaN transistors should be driven with 5 V. The temperature coefficient of $R_{DS(on)}$ of the GaN transistor is also similar to the silicon MOSFET as it is positive. The magnitude is significantly less. The 125˚C point is 1.45 times the 25˚C point for the EPC1001 compared to 1.7 for silicon. This advantage increases with increasing voltage.

Capacitance

In addition to the low $R_{DS(on)}$, the lateral structure of the GaN transistor makes it a very low charge device as well. It has the capability of switching hundreds of volts in nanoseconds, giving it multiple megahertz capability. This capability will lead to smaller power converters, and higher fidelity class D amplifiers. Most important in switching is C_{GD}. With the lateral structure, C_{GD} comes only from a small corner of the gate. An extremely low C_{GD} leads to the very rapid voltage switching capability of GaN transistors.

C_{GS} consists of the junction from the gate to the channel, and the capacitance of the dielectric

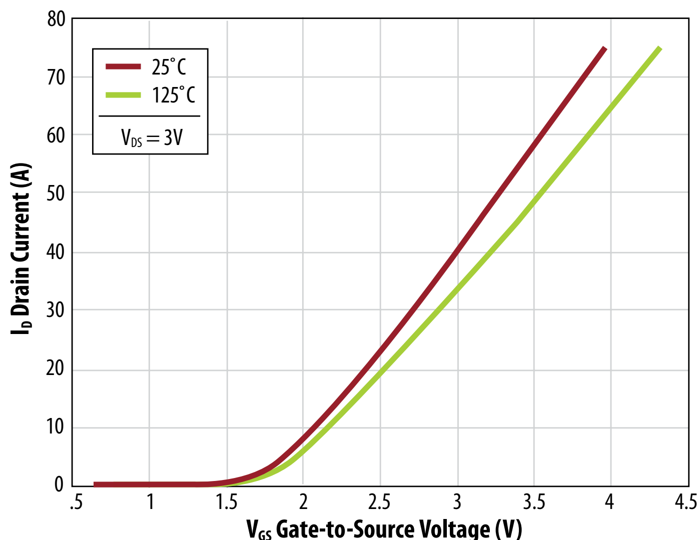


Figure 3: Transfer characteristics curve

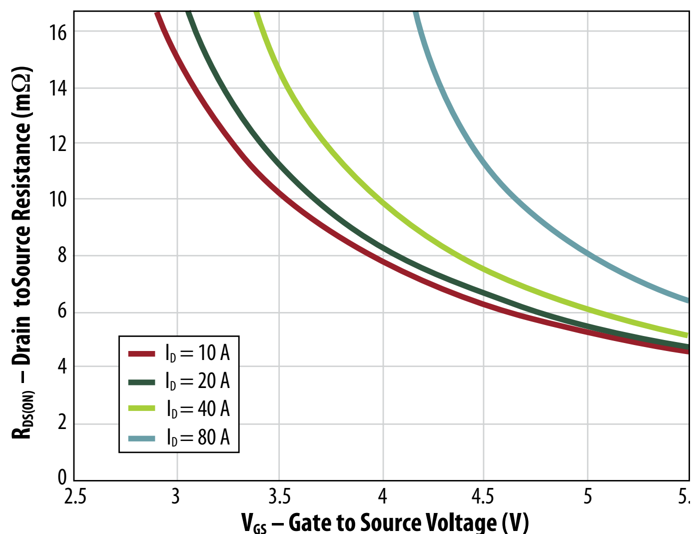
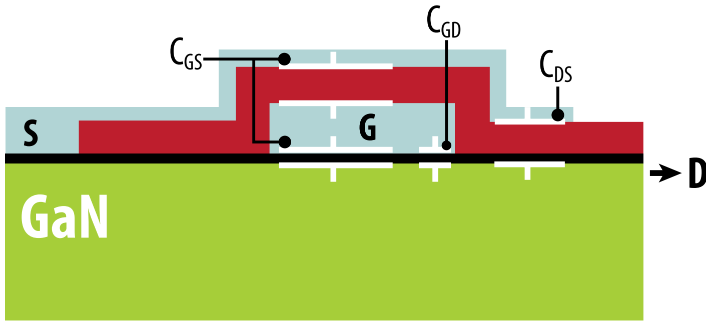


Figure 4: $R_{DS(on)}$ versus VG at various currents



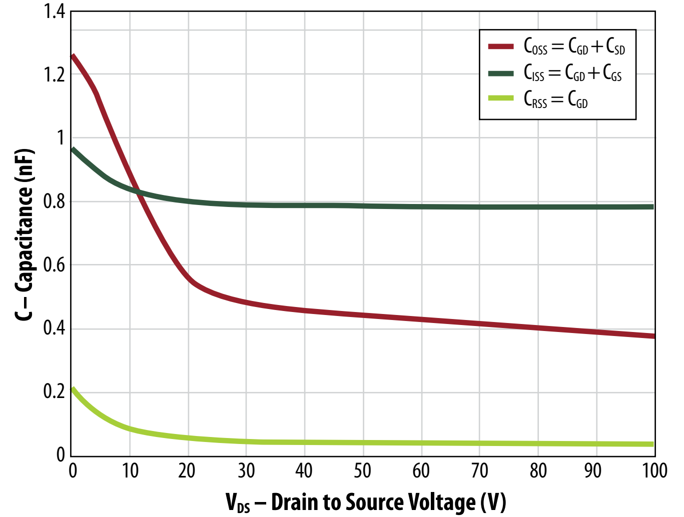


Figure 5 (above): Physical capacitance locations

Figure 6 (right): Capacitance curves, EPC1001

between the gate and the field plate. CGS is large when compared with C_{GD}, giving GaN transistors excellent dV/dt immunity, but still small when compared with Silicon MOSFETs giving them very short delay times, and excellent controllability in low duty cycle applications. A 48 V to 1V buck regulator has been demonstrated at 1 MHz using 100 V GaN transistors from EPC. C_{DS} is also small, being limited to the capacitance across the dielectric from the field plate to the drain. Physical capacitance locations are shown in figure 5. Capacitance versus Voltage curves for GaN again look similar to those for silicon except that for with a similar resistance, its capacitance is significantly lower and flattens out much sooner. Capacitance curves for the EPC1001 are shown in figure 6.

Series Gate Resistance and leakage

Series Gate Resistance (RG) limits how quickly the capacitance of a Field Effect Transistor can be charged or discharged. Silicon MOSFETs are limited to using Polysilicon or Silicide where GaN transistors use metal gates. The metal gates enable GaN to have gate resistances of a couple tenths of an ohm. This low gate resistance also helps with dV/dt immunity.

For isolating the gate, oxide growth is not an option with GaN. For this reason, the gate leakage current of GaN transistors is higher than that of Silicon MOSFETs. Designers should expect gate leakage on the order of 1 mA. As these are low gate drive voltage devices, losses associated with gate leakage are low.

Figure of Merit

Total Gate Charge (Q_G) is the integral of C_{GS} plus C_{GD} over Voltage. A common figure of merit that takes both on state and switching performance into account is ($R_{DS(on)}$ x Q_G). Figure of merit for GaN transistors versus best in class silicon MOSFETs are presented in figure 7 for 100 V devices and figure 8 for 200 V devices.

Body Diode

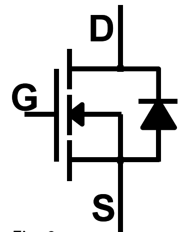


Fig. 9

The last part of the performance picture is that of the so-called "body diode". As seen from figure 1, EPC's GaN transistor structure is a purely lateral device, absent of the parasitic bipolar junction common to Silicon based MOSFETs. As such, reverse bias or "diode" operation has a different mechanism but similar function. With zero bias gate to source, there is an absence of electrons under the gate region. As the drain voltage is decreased, a positive bias on the gate is created relative to the drift region, injecting electrons under the gate. Once the gate threshold is reached, there will be sufficient electrons under

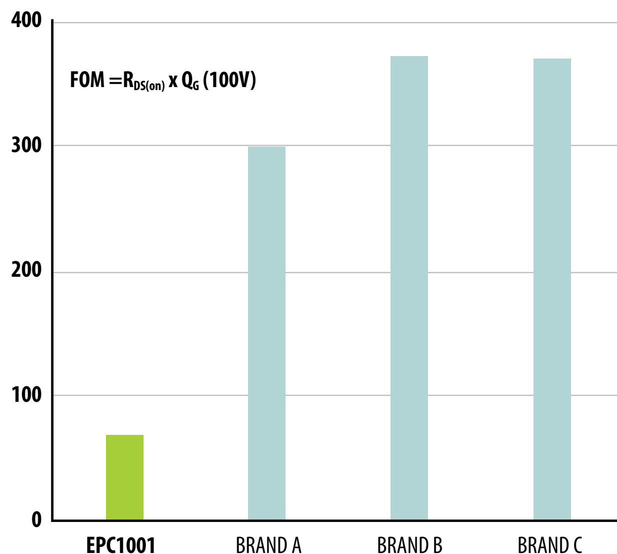


Figure 7

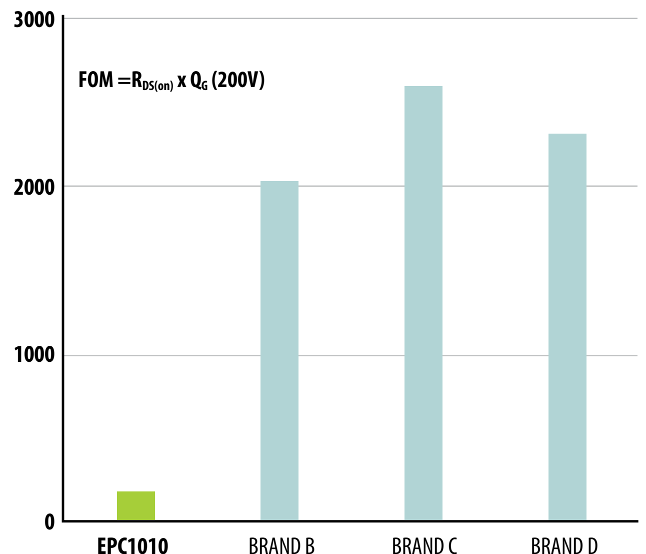


Figure 8

the gate to form a conductive channel. The benefit to this mechanism is that there are no minority carriers involved in conduction, and therefore no reverse recovery losses. While Q_{RR} is zero, output capacitance (C_{OSS}) has to be charged and discharged with every switching cycle. For devices of similar $R_{DS(on)}$, GaN transistors have significantly lower C_{OSS} than silicon MOSFETs. As it takes threshold voltage to turn on the GaN transistor in the reverse direction, the forward voltage of the "diode" is higher than silicon transistors. As with silicon MOSFETs, care should be taken to minimize diode conduction.

As fundamental operation of GaN transistors is similar to that of silicon MOSFETs, they can be represented schematically the same way as shown in figure 9.

Packaging

EPC's GaN transistors are insulated from the substrate. This allows monolithic fabrication of multiple transistors in any configuration and efficient, common heatsinking without the need for an insulating layer between the device and the heatsink. It also forces the current for both drain and source to be collected on one side of the die. To keep the resistance low in the metal layers that collect the current, these paths must be kept short. To accomplish this, wafer level line grid arrays are used where Drain and Source lines are alternated. Standard line pitches are 0.4 mm and 0.6 mm. Figure 10 shows the EPC1010, a 200 V, 25 mΩ transistor. Where this does not allow compliance with safety agency creepage distance requirements, underfill can be used.

Figure 10

Applications and Value

EPC brings enhancement mode to GaN. This allows immediate realization of the disruptive gains in efficient high frequency and low duty cycle power conversion. Other "exotic" technologies are either cost prohibitive or use depletion mode. Depletion mode devices lose control when there is no power, and require new development in control ICs.

GaN transistors will bring a leap in Class D audio technology by enabling efficient switching at frequencies above the AM band. Fidelity will approach Class A and Class AB systems without all of the size and weight limitations of linear amplifiers. They will allow high quality amplifiers to be built into very tight spaces such as flat screen televisions, computers and speakers.

In information processing and storage systems, the whole power architecture can be reevaluated to take advantage of the outstanding switching capabilities. As output voltage increases for AC/DC converters, efficiency goes up. As bus voltage increases, transmission efficiency goes up. As frequency increases, size goes down. EPC GaN enables the last stage which enables the first two while increasing AC/DC efficiency when used as synchronous rectifiers. They also allow for intermediate stage converters to be removed for single step conversion, saving the size and cost of the intermediate stage converter.

Conclusion

EPC Gallium Nitride transistors bring tremendous performance and size advantages over silicon. These advantages can be applied to gain efficiency advantages, size advantages, or a combination of both, with application requirements and a cost structure that are similar to silicon. To take full advantage of GaN, power architects should rethink their system. The future of GaN transistors is now.